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Utility Patent Application Transmittal (Only for new non-provisional applications Under 37 CFR 1.53(b))

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Washington, D. C. 20231

Case Docket No.0325.00339
Date: May 24, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Timothy J. Williams

For: ADJUSTABLE MICROCONTROLLER WAKE-UP SCHEME

Enclosed are:

1. Specification (18 pages); Claims (5 pages); Abstract (1 page)
2. 3 sheets of formal drawings.
3. Oath or Declaration Total Pages 2
 - a. Newly executed (original or copy)
 - b. Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Item 5 completed)
 - c. Copy of Revocation of Previous Power
4. Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
5. If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

 Continuation Divisional Continuation-in-part (CIP)
of prior application no.: _____

6. An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.
7. A PTO Form 1449 with a copy of the references not previously cited.
8. Return Receipt Postcard
9. Other:

The filing fee has been calculated as shown below:

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Basic Fee	--	--	--	\$690.00
Total Claims	20	0	x \$ 18.00	\$ 0.00
Indep. Claims	3	0	x \$ 78.00	\$ 0.00
Mult. Dep. Claims			\$260.00	\$ 0.00

SUB-TOTAL \$690.00

SMALL ENTITY STATUS (divide SUB-TOTAL by two) \$
 Assignment Recordal Fee (\$40.00) \$ 40.00
 TOTAL \$730.00

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CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL561050724US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on May 24, 2000.

By: Mary Donna Berkley
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Respectfully submitted,

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ADJUSTABLE MICROCONTROLLER WAKE-UP SCHEMEField of the Invention

The present invention relates to a method and/or architecture for wake-up schemes generally and, more particularly, to a method and/or architecture for an adjustable microcontroller wake-up scheme.

Background of the Invention

Conventional methods and/or circuits for wake-up schemes are based on a fixed delay element. The fixed delay element is implemented either on-chip or off-chip. One such conventional method implements an R-C charging circuit configured to cause the wake-up event (e.g., generation of an interrupt). Another such conventional method implements a free-running low power oscillator.

Conventional off-chip timers (i) require additional pins on the microcontroller device and (ii) require external components (e.g., R-C charging circuit). Conventional on-chip timers (i) are not accurate, (ii) lack a mechanism to improve accuracy, (iii) require several cycles of wake-up and re-suspend for long delays

and (iv) have high power consumption. Additionally, both off-chip and on-chip timers have limited wake-up time ranges.

Summary of the Invention

5 The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to wake-up the second circuit in response to an input signal. The input signal generally comprises a programmable delay value.

10 The objects, features and advantages of the present invention include providing a method and/or architecture for implementing a wake-up scheme that may (i) provide an internal solution for causing the wake-up of microcontrollers by moving from a suspend or sleep mode, (ii) implement relatively long target times (e.g., up to hundreds of milliseconds or more), (iii) implement a range of wake-up times and/or (iv) provide increased accuracy.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

5 FIG. 1 is a block diagram of a preferred embodiment of the present invention;

FIG. 2 is a detailed block diagram of a divider circuit of FIG. 1;

10 FIG. 3 is a block diagram of an alternate embodiment of the present invention; and

FIG. 4 is a block diagram of an implementation of the present invention.

Detailed Description of the Preferred Embodiments

15 Referring to FIG. 1, a block diagram of circuit 100 is shown in accordance with a preferred embodiment of the present invention. In one example, the circuit 100 may be implemented as a user programmable wake-up timer. The circuit 100 may implement a programmable wake-up timer that may be used with a processing 20 device, such as a microprocessor or a microcontroller, to control the exiting of a suspend or sleep mode. The circuit 100 may also

allow variations in the wake-up time (that may result from processing or operating conditions) to be tuned out. The circuit 100 may allow a user to program a delay value for a wake-up operation. The timer 100 may have a low-power consumption and may 5 operate in a low-power suspended state without requiring any additional pins or external components.

The circuit 100 may be required to provide a periodic wake-up indication. The circuit 100 may be required to provide the periodic wake-up indication to allow a device (e.g., a computer) to respond to an event (e.g., push of a button or mouse movement). A timing of the wake-up indication may be programmed by a user. The circuit 100 may allow for significant variation and/or adjustment of the wake-up time for different users/applications. The circuit 100 may provide a reasonable accuracy in sleep time (e.g., 15 efficient use of suspend mode power budget). In the example of a Universal Serial Bus (USB) microcontroller, an average current of less than 500 uA during suspend may be implemented. However, other suspend currents may be implemented accordingly to meet the design criteria of a particular implementation. Additionally, the circuit 20 100 may be configured to operate between two operating modes. For example, the circuit 100 may operate under any power conditions

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between a full operation mode and a sleep (or suspend) operation mode (e.g., between (i) a low speed/high speed mode, (ii) a low power/high power mode, etc.). The circuit 100 may eliminate pins previously used for external wake-up components.

5 The structure of the circuit 100 may comprise a delay block (or circuit) 102, a divider block (or circuit) 104 and a multiplexer block (or circuit) 106. In one example, the divider block 104 and the multiplexer block may be implemented as a single select block (or circuit). The delay block 102 may have an input 108 that may receive a signal (e.g., ENABLE). Additionally, the delay block 102 may have an output 110 that may generate a signal (e.g., DELAY). The signal ENABLE may initiate the generation of the signal DELAY by the delay block 102. The signal DELAY may be presented to an input 112 of the divider block 104.

15 The divider block 104 may have an output 114 that may generate n number of signals (e.g., DIV_DEL), where n is an integer. The signals DIV_DEL may be implemented, in one example, as divided delay signals. The divided delay signals DIV_DEL may be presented to an input 116 of the multiplexer 106. The multiplexer 20 106 may have an input 118 that may receive a signal (e.g., ADJUST[3:1]). In one example, the signal ADJUST[3:1] may be

implemented as a multi-bit signal. In another example, the signal ADJUST[3:1] may be implemented as a user programmable input signal.

The multiplexer 106 may have an output 120 that may generate a signal (e.g., OUTPUT). In one example, the signal 5 OUTPUT may be implemented as a wake-up signal. However, the signal OUTPUT may be implemented as another appropriate signal in order to meet the criteria of a particular implementation. The multiplexer 106 may multiplex the divided delay signals DIV_DEL in response to the signal ADJUST[3:1]. The circuit 100 may provide an internal timer with range selection and calibration capability.

In one example, the delay block 102 may be implemented as an analog delay circuit. In another example, the delay circuit 102 may be implemented as a current charging a capacitor, a ring oscillator, and/or a R-C delay time. However, the delay block 102 may be implemented as other types delay devices in order to meet the criteria of a particular implementation. The delay circuit 102 may be implemented as a slow-charging circuit having minimal power consumption. The delay 102 may be configured to provide a baseline delay time (e.g., the signal DELAY). The signal DELAY and 15 therefore the delay time of the circuit 100 may typically have a wide variation in an integrated circuit application. The variation 20

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of the signal DELAY is generally dominated by silicon processing variations in the fabrication of the integrated circuit containing the circuit 100.

Referring to FIG. 2, a detailed block diagram of the 5 divider block 104 is shown. The divider block 104 generally comprises a number of divide blocks (or circuits) 130a-130n. The divide blocks 130a-130n may be implemented, in one example, as divide by 2 dividers. However, the divide blocks 130a-130n may each be implemented as another appropriate divider in order to meet the criteria of a particular implementation. The divide blocks 130a-130n may be connected in series. The divide block 130a may receive the signal DELAY. The divide block 130a may present a divided output signal to the divide block 130b. Each of the divide blocks 130b-130n may receive a divided output from a proceeding 15 divide block 130a-130n.

Additionally, each of the divide blocks 130a-103n may be connected to the divided delay signal DIV_DEL. Each of the divide blocks 130a-130n may be configured to generate at least one divided clock signal of the divided delay signal DIV_DEL. The divided 20 clock signals may be presented as the divided delay signal DIV_DEL.

The divider circuit 104 may be implemented to extend a delay range of the circuit 100. The divider block 104 may divide the signal DELAY into the multiple divided signals DIV_DEL. In one example, the divider 104 may be implemented as a ripple divider circuit. However, the divider circuit 104 may be implemented as other appropriate delay devices in order to meet the criteria of a particular implementation. The multiplexer 106 may multiplex the divided delay signals DIV_DEL in response to the signal ADJUST[3:1]. The multiplexer 106 may tune the signal OUTPUT in response to the signal ADJUST[3:1].

The signal ADJUST[3:1] may be implemented, in one example, as a 3-bit signal. However, the signal ADJUST[3:1] may be implemented as other appropriate bit-width signals to meet the criteria of a particular implementation. The circuit 100 may provide a number of wake-up times (e.g., the multiple delay signals DIV_DEL) with respect to an initial delay time (e.g., the signal DELAY). The signal ADJUST[3:1] may allow the number of the wake-up times. The wake-up timer of the circuit 100 may be programmed by the signal ADJUST[3:1]. However, the circuit 100 may be programmed in a number of alternate ways such as (i) pins configured to store a delay value, (ii) data pins configured to receive a delay value,

(iii) loading in a delay value from a register, (iv) coding a delay value in microprocessor code, and/or (v) coding a delay value in firmware. However, the circuit 100 is not limited to the programming methods as described.

5 The circuit 100 may tune out variation from process (and possibly operating conditions). The circuit 100 may allow a processor to automatically choose a range closest to a target sleep period (via the signal ADJUST[3:1]).

10 In general, once the signal ENABLE is asserted, the delay block 102 may generate the signal DELAY. The signal DELAY is generally presented to the divider block 104. The divider 104 may present the divided delay signals DIV_DEL to the multiplexer 106. The multiplexer 106 may generate the signal OUTPUT in response to the signal ADJUST[3:1] and the signals DIV_DEL. The signal ADJUST[3:1] may allow configuration of a number of delay counts of 15 the circuit 100. The signal OUTPUT may be implemented as a wake-up signal (e.g., an interrupt) to bring the device out of sleep or suspend mode.

20 The various signals are generally "on" (e.g., a digital HIGH, or 1) or "off" (e.g., a digital LOW, or 0). However, the particular polarities of the on (e.g., asserted) and off (e.g., de-

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asserted) states of the signals may be adjusted (e.g., reversed) accordingly to meet the design criteria of a particular implementation.

The wake-up time is generally adjusted by a programmable number of control bits of the signal ADJUST[3:1]. The number of, as well as the control bits themselves, may be programmed by a user or by appropriate firmware. In one example, the number of control bits may be 3. However, other numbers of control signals may be implemented accordingly to meet the design criteria of a particular implementation. In the example of 3 control bits, 8 possible wake-up times may be implemented. Each of the 8 choices of wake-up times, in one example, may increase the delay time by a factor of 2 times longer than the time delay of the previous setting. For example, the wake-up delay times may have settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, and 128x greater than the default delay. The default delay is typically a convenient wake-up time and/or the fastest wake-up time allowable.

In one example, a default delay time of 3 ms may be defined. Operating condition delays of the device typically vary between 1 ms and 5 ms from the baseline delay (e.g., 3 ms) of a particular chip. To generate a 100 ms delay, the 32x choice

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generally provides $3 * 32$, or 96 ms nominal delay. However, the 32x choice may provide a delay range that may vary between 32 ms and 160 ms. For applications such as a wake-up from suspend (e.g., in USB mouse applications), the delay time is generally controlled as accurately as possible. The tuning scheme (e.g., programming) of the timer 100 may allow the delay of the circuit 100 to be tuned to within $\pm 35\%$ of the desired delay range. Typical representative default wake-up times are shown in TABLE 1 below. The setting column may show different configurations of the signal ADJUST[3:1].

TABLE 1

Setting	Wake-up scale	Min Time (ms)	Max Time (ms)
1	1x	1	5
2	2x	2	10
3	4x	4	20
4	8x	8	40
5	16x	16	80
6	32x	32	160
7	64x	64	320
8	128x	128	640

For a 100 ms desired delay time, the useful range choices may be implemented by tuning to the best range. A predefined limit (e.g., between 64 ms and 128 ms or between setting 7 and 8) may represent a fastest condition or a predefined limit (e.g., between 80 ms and 160 ms or between settings 5 and 6) may represent a slowest condition. By selecting an optional setting (e.g.,

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settings 1-8) for a particular device, the wake-up time error in a worst case scenario is normally less than $\pm 35\%$ from the desired time.

The wake-up time of the timer 100 may be tuned (e.g., programmed) by the signal ADJUST[3:1]. Additionally, the wake-up time for a device may be measured during a normal operation (e.g., non-suspended). The measurement of the wake-up time for a particular chip may be accomplished by (i) determining an initial wake-up setting, (ii) starting the wake-up timer 100 (which runs in either awake or suspended modes), (iii) determining a delay time between enabling the wake-up timer 100 and an assertion of the signal OUTPUT and (iv) changing the initial wake-up setting in response to the delay time. The measured wake-up time may indicate a speed of the chip (under the current conditions). The timer 100 may allow a user and/or appropriate firmware to select the best wake-up setting for the particular chip. The wake-up setting may be stored in a register and presented to the signal ADJUST[3:1] during suspend mode (if the circuit is enabled).

The wake-up time determination scheme may be repeated to account for changes in operating conditions. The timer 100 may implement alternate scale factors to the geometric wake-up scale

5 factors (1x, 2x, ... 128x). However, the alternate scale factors may have to trade-off range for resolution. For example, the scale factors may be increased to cover a greater range with a predetermined number of bits (e.g., 1x, 4x, 16x, 64x ...).
10 However, the greater range has a trade-off of reduced resolution and accuracy.

15 Referring to FIG. 3, a block diagram of an alternate embodiment of the present invention marked with primed notation is shown. The circuit 100' may be similar to the circuit 100. The circuit 100' generally comprises the delay block 102' and a counter block (or circuit) 140. The delay block 102' may have the output 110' that may present the signal **DELAY**. The signal **DELAY** may be presented to an input 142 of the counter 140. An input 144 of the counter 140 may receive the signal **ADJUST[3:1]**. Additionally, the counter 140 may have an output 146 that may present the signal **OUTPUT**. In one example, the counter 140 may be implemented as a down counter. In another example, the counter 140 may be implemented as an up counter. However, the counter 140 may be implemented as another appropriate type or configuration of counter
20 in order to meet the criteria of a particular implementation.

The delay circuit 102' may clock the counter 140. The delay counter 102' may clock the counter with the delay clock DELAY. An initial count of the counter 140 may be provided by the signal ADJUST[3:1]. The counter 140 may count UP/DOWN in response 5 to the signal DELAY and the signal ADJUST[3:1]. The counter 140 may count from the initial value determined from the signal ADJUST[3:1]. The initial value of the signal ADJUST[3:1] may be programmed. Additionally, the initial value may be programmed by a user. When the counter 140 reaches a predetermine value determined by the signal ADJUST[3:1], the counter 140 may assert the signal OUTPUT. For example, the counter 140 may start from an initial value determined by the signal ADJUST[3:1] and count up/down to a target value (e.g., 0 or 7). Additionally, the counter 140 may start from an initial value (e.g., 0 or 8) and 10 count up/down to a target value determined by the signal ADJUST[3:1].

The counter 140 may reload to the initial count value each time the counter 140 counts to the predetermined value. The circuit 100' may allow delay time selections to be linear (e.g., 1x, 2x, 3x, 4x, etc.). The circuit 100' may provide increased 20 resolution (e.g., smaller step size). However, the circuit 100'

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may provide a smaller total delay range for a given number of input signals.

The tuning scheme (e.g., programming) of the timer 100 may allow the delay of the circuit 100' to be tuned to within $\pm 30\%$ of the desired delay range. Typical representative default wake-up times are shown in TABLE 2 below. The setting column may show different configurations of the signal ADJUST[3:1].

TABLE 2

Setting	Wake-up scale	Min Time (ms)	Max Time (ms)
1	1x	1	5
2	2x	2	10
3	3x	3	15
4	4x	4	20
5	5x	5	25
6	6x	6	30
7	7x	7	35
8	8x	8	40

For a 7.5 ms desired delay time, the useful range choices may be implemented by tuning to the best range. A predefined limit (e.g., between 7 ms and 8 ms or between setting 7 and 8) may represent a fastest condition or a predefined limit (e.g., between 5 ms and 10 ms or between settings 1 and 2) may represent a slowest condition. By selecting an optional setting (e.g., settings 1-8) for a particular device, the wake-up time error in a worst case scenario is normally less than $\pm 30\%$ from the desired time.

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Referring to FIG. 4, an implementation of the timer 100 (or 100') is shown. In one implementation, the timer 100 may be implemented within a controller 200. The controller 200 may be implemented as, in one example, a microcontroller. However, the controller 200 may be implemented as other appropriate type device in order to meet the criteria of a particular implementation. The timer 100 may operate internally to the microcontroller 200. The microcontroller 200 may provide the signal ENABLE and the signal ADJUST[3:1]. Additionally, the microcontroller 200 may receive the signal OUTPUT. The signal OUTPUT may be implemented as a wake-up signal for the microcontroller 200.

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The timer 100 may implement, in one example, a fully internal wake-up timer (e.g., a timer within a microcontroller that does not require additional pins or external devices to operate). The wake-up timer 100 may retain a wide range of wake-up times and provide accurate tuning of the wake-up times. Additionally, the timer 100 may provide an area efficient circuit with low power consumption.

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The wake-up timer 100 may be implemented in circuits, such USB microcontrollers, to solve conflicting demands over desired wake-up times. However, the wake-up timer 100 may be

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implemented in a number of design implementations. For example, the delay circuit 102 may be implemented as any type of low power oscillator circuit to provide an appropriate base delay of a particular implementation. Additionally, the timer 100 may be 5 auto-calibrated by appropriate firmware to select an accurate target delay time.

The function performed by the timer 100 of FIGS. 1 and 3 and 4 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will also be apparent to those skilled in the relevant art(s).

15 The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a device to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of ROM, RAM, EPROM, EEPROM, Flash memory, 20 or any type of media suitable for storing electronic instructions. The present invention may also be implemented by the preparation of

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ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

5 While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a first circuit configured to wake-up a second circuit in response to an input signal, wherein said input signal comprises a
5 programmable delay value.

2. The apparatus according to claim 1, wherein said

input signal comprises a user programmable signal.

3. The apparatus according to claim 1, wherein said

input signal comprises a multi-bit signal.

4. The apparatus according to claim 1, wherein said

delay value comprises a programmable delay value.

5. The apparatus according to claim 1, wherein said

delay value comprises a wake-up timing value.

6. The apparatus according to claim 1, wherein said

first circuit comprises:

a delay circuit configured to present a first delay signal; and

5 a select circuit configured to present a second delay signal in response to said first delay signal, wherein said second delay signal is configured to wake-up said second circuit.

7. The apparatus according to claim 6, wherein said input signal is configured to control a programmable delay of said second delay signal.

8. The apparatus according to claim 7, wherein said programmable delay comprises a multiple of said first delay signal.

9. The apparatus according to claim 6, wherein said select circuit is further configured in response to said input signal.

10. The apparatus according to claim 6, wherein said select circuit comprises:

a divider circuit configured to present one or more divided signals in response to said first delay signal; and

5 a multiplexer configured to present said second delay signal in response to said one or more divided signals and said input signal.

11. The apparatus according to claim 6, wherein said select circuit comprises a counter configured to generate said second delay signal in response to said input signal.

12. The apparatus according to claim 6, wherein said delay circuit is further configured to present said delay signal in response to an enable signal.

13. The apparatus according to claim 1, wherein said input signal is generated in response to a device selected from the group consisting of input pins, data pins, microprocessor code, and firmware.

14. An apparatus comprising:
a first circuit configured to operate in a first mode or a second mode; and

5 a second circuit configured to control switching of said
first circuit from said first mode to said second mode after a
programmable period of time.

15. A method for wake-up timing comprising the steps of:

- (A) receiving an input signal; and
- (B) waking-up a circuit in response to said input signal,

wherein said input signal comprises a programmable delay value.

16. The method according to claim 15, wherein said input signal comprises a user programmable signal and said delay value comprises a programmable delay value.

17. A computer readable medium containing instructions to execute the steps of claim 15.

18. The method according to claim 15, wherein step (B) further comprises the sub-steps of:

- (B-1) presenting a first delay signal; and

5 (B-2) presenting a second delay signal in response to
said first delay signal, wherein said second delay signal is
configured to wake-up said circuit.

19. The method according to claim 18, wherein step (B)
further comprises the sub-step of:

(B-3) controlling a programmable delay of said second
delay signal.

20. The method according to claim 15, further comprising
the step of:

(C) generating said input signal in response to input
pins, data pins, microprocessor code, and/or firmware.

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ABSTRACT OF THE DISCLOSURE

An apparatus comprising a first circuit and a second circuit. The first circuit may be configured to wake-up the second circuit in response to an input signal. The input signal generally comprises a programmable delay value.

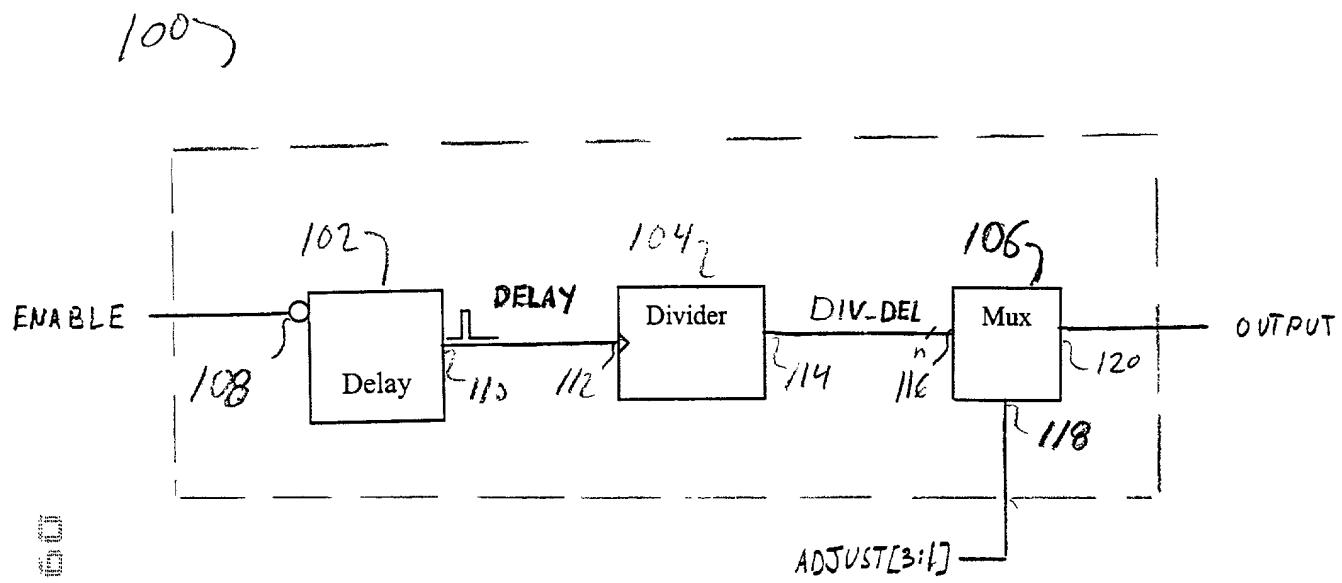


FIG.1

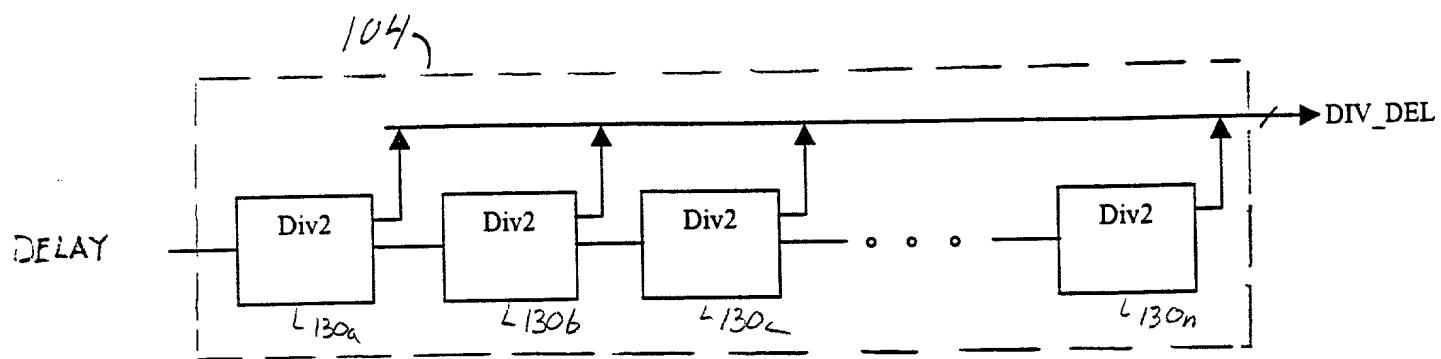


FIG.2

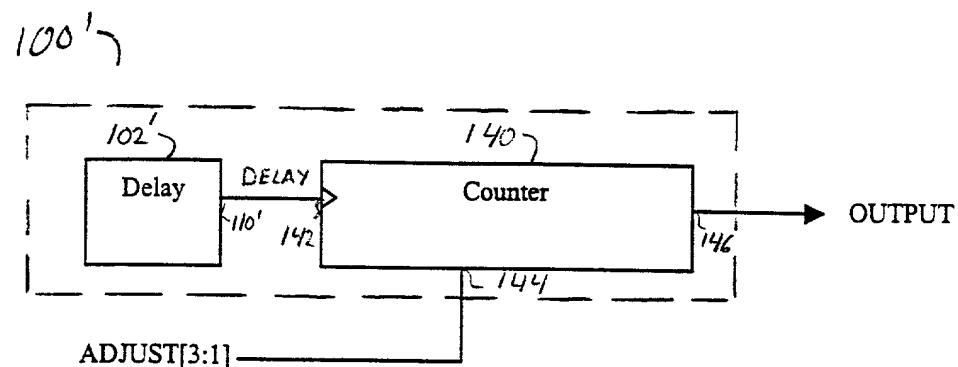


FIG.3

200>

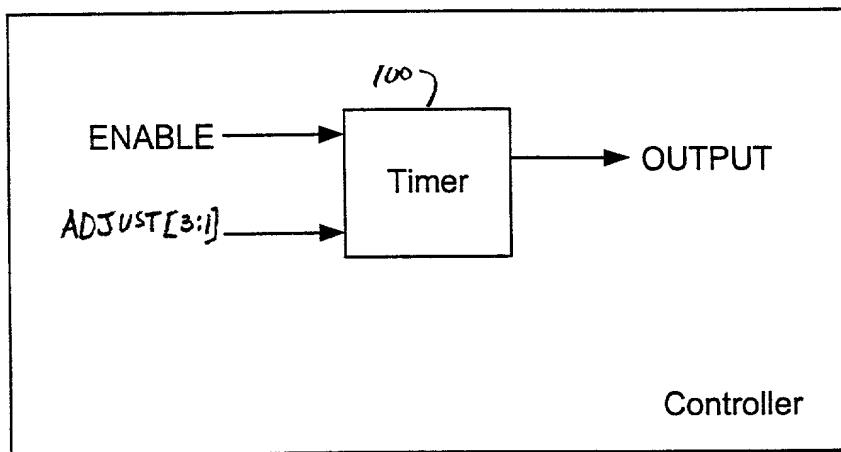


FIG.4

DECLARATION, POWER OF ATTORNEY AND PETITION

I, the undersigned inventor, hereby declare that:

My residence, post office address and citizenship are given next to my name;

I believe that I am the first, original and sole inventor of the subject matter claimed in the application for patent entitled "**ADJUSTABLE MICROCONTROLLER WAKE-UP SCHEME**", which:

X is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

I have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

I acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. I also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or

refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

I hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.

Filing Date

I hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.

Filing Date

Status

I hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, I acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

I hereby appoint as my attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

**21363**

PATENT TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

Timothy J. Williams

Inventor

Timothy J. Williams

Signature of Inventor

5/22/00

Date

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